Residual Current Detection Device

This invention relates to a residual current correction device for use in a circuit breaker.

Conventionally, residual current correction is detected utilising a current transformer having primary windings through which, in the case of a single phase device, load current flows in opposite directions so that if the return current is different from the outwardly flowing current because of current leakage an output voltage signal is induced in a secondary winding of the transformer. In the case of a multi-phase device, primary windings of the transformer are connected in all of the phase lines and the neutral line. In normal situations, when there is no current leakage, the net current in the lines is zero so that no output voltage is zero.

Sophisticated materials have been developed for the core of the current transformer, which enable considerable accuracy to be obtained when the currents flowing in the primary windings are substantially sinusoidal. However, switch mode power supplies are often used for computers and other equipment and there is an increasing tendency for such equipment to cause dc offsets in the currents. Such developments have made detectors utilising current transformers less reliable and prone to false tripping or failure to detect a dc current leak.

This is a particular problem in the case of directly actuated electro-mechanical devices, where the current transformer secondary actually drives an actuator. The situation is not much improved, when by including an electronic detection and amplification means connected to the secondary winding, as there are still problems with high frequency transients and dc offsets. A very small dc current level can cause the core

to saturate thereby seriously impairing the ability of the detector to detect current leakage.

It is an object of the present invention to provide a residual current detection device in which the above mentioned problems are substantially overcome in a simple and efficacious manner.

In accordance with the invention there is provided a residual current detection device comprising a plurality of resistive shunts for connection in respective ones of a plurality of lines though which current can flow to and from a load, and detector means sensitive to the voltage developed across each of the shunts to detect any imbalance between the currents flowing though the shunts.

Preferably, the detector means comprises an analog to digital converter for each shunt and a processor for receiving the digital signals from the converters and determining whether a current imbalance exists.

Each shunt preferably takes the form of a composite strip having conductive portions at its ends and a resistive portion interconnecting the conductive portions. Such composite strips can be mass produced inexpensively to very high tolerances which makes them extremely suitable for this purpose.

The analog to digital converter for each shunt may include a delta-sigma modulator, which generates a high frequency single digital data stream which is converted by decimation filtering to a multibit digital data stream at a lower frequency.

The analog to digital converter for each shunt is preferably connected to

the processor through an isolation barrier so that the converter can float at the voltage level of the shunt which it serves. The decimation filtering may be effected entirely in the converter, entirely in the processor or split between the converter and the processor.

In the accompanying drawings:

Figure 1 is a diagrammatic perspective view of an example of the invention as applied to a single phase device and

Figure 2 is a block diagram of an another example of the invention as applied to a three phase device.

In the device shown in Figure 1, a substrate 10 supports two composite conductor strips 11, 12. Each of these includes end portions 13 of copper and an intermediate portion 14 of a resistive material such as manganin. The strips are formed by slicing up a sandwich formed by electron beam welding the copper portions to opposite sides of the manganin portion. The shunts formed by the resistive portions manufactured by this method can have a nominal resistance of 0.2mΩ to a tolerance of less than 5%. If the two shunts 14 used on one device are pressed from adjacent portions of the sandwich stock, they are matched to within 2%. Calibration of the shunts built into a unit at two different temperatures can virtually eliminate shunt errors.

In the example shown in Figure 1, there is a separate signal pre-processing ASIC 15 mounted on each of the shunts 14 and connected to the copper end portions 13 of the associated conductor strips. The two ASICs 15 are connected to via an isolation transformer array 16 to a main processor 17. The ASICs 15 operate to convert the two voltages across the shunts into a

digital signal stream which is communicated to the processor 17 via the isolation transformer array. The main processor is programmed to provide a drive signal to a trip actuator 18.

Figure 2 shows in rather more electrical detail a three phase device. In this case there are four shunts 14, one in each phase line and a fourth in the neutral line. The ASICs 15 of Figure 1 are shown as four separate blocks 20, 21, 22, and 23, and there is a power supply unit 24 which draws power from the phase lines on the mains side of the shunts 14 and provides controlled voltages to the processor 17. Power is supplied to the four blocks 20 to 23 via isolation barriers 25 which make up the array 16. Each block of the ASIC includes an analog to digital converter in the form of a delta-sigma modulator which provides a high frequency one bit digital data stream. A multiplexer may be included in each converter so that the converter can provide to the processor, through the respective isolation barrier, signals representing both current in the associated shunt and the voltage at one end of it. The processor uses these signals to monitor the current in each shunt and to operate the actuator 18 if an imbalance occurs.

It will be noted that the voltage sensing connections to the ASICs are made via resistor chains connected between each phase line and the neutral. Each such resistor chain comprises an outer pair of precision resistors of relatively low ohmic value and an intermediate resistor of relatively high ohmic value. These resistor chains allow the RCD to be provided with an independent reference. If the neutral ADC is taken as the selected system reference, then the operating software of the main processor can use the multiple signals derived from the several resistor chains to calibrate each phase against the neutral reference.

The CPU is programmed to carry out the necessary calculations to determine the existence of an imbalance and can determine the true RMS value of the residual current, which conventional devices fail to do correctly particularly in the case of non-sinusoidal current waveforms. The CPU may be programmed to enable it to determine from the data it receives whether a particular event is, in fact, an unacceptable leakage more reliably than conventional devices. For example, the CPU can take into account the historic performance of the unit when setting the leakage current threshold and may ignore events which have a recognisable "signature". In this way improved tolerance to nuisance tripping can be obtained

Decimation filtering of the high frequency one bit data stream is required to reduce each data stream to a multi-bit digital signal at a predetermined sample frequency. By way of example, each current signal may be a 23-bit signal at a sample rate of 64 times the mains frequency, but lower resolution at lower sample rates can be employed when non-linear, rather than linear conversion is acceptable. The decimation filtering is typically a function of the processor, filtering of the four data streams being executed simultaneously so that sample values are derived for all four shunts simultaneously.

In alternative embodiments, one or more stages of the decimation filtration may be executed by hardware included within the ASIC. Multi-bit digital words are transmitted serially across the isolation barriers instead of a one-bit signal stream.

The arrangements described enable very accurate detection of current imbalance to be effected even in the presence of switching transients and DC offsets. The problems which arise from potential saturation of the

current transformer core are avoided completely.

Since the CPU receives actual line current and voltage data from each of the blocks 20 to 23, it can be programmed to perform other calculations, such as current limit and power consumption. Thus an RCD device constructed as described above can also provide the functions of a conventional circuit breaker and/or those of a power consumption meter without any additional sensing or analog-to-digital components being required.